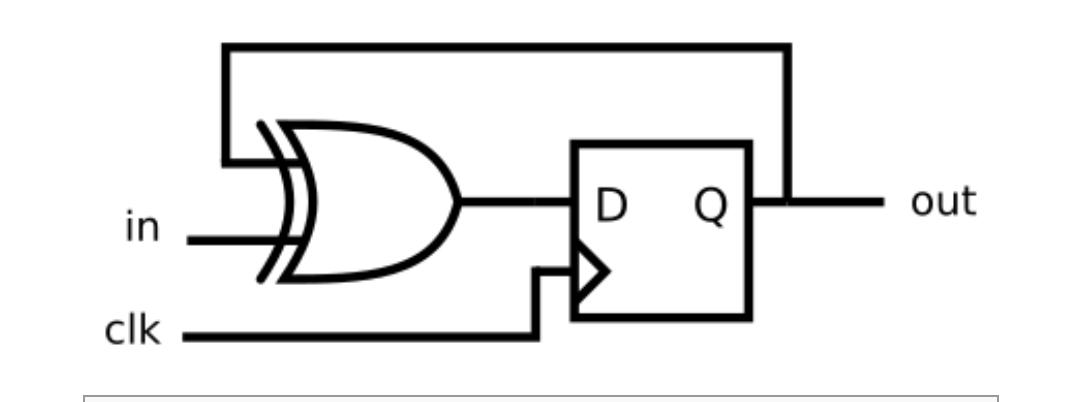
ASSIGNMENT-3

Code the following on verilog and test them using the testbench file. You have to submit both the module (**m**) file and the testbench (**tb**) file. Follow up:

1. Save each file as **RollNo\_A3\_Q{x}\_y** where (1<=x<=8) and y = {m, tb}
2. Deadline is Sunday EOD 05/01/2025
3. **Attach all the files in a drive link and submit it along with view access** [**https://docs.google.com/forms/d/e/1FAIpQLSe7V92eMLFGL6DMX\_rz3r1WhvPmD\_am9ON-VkE5OfJIDZvbxw/viewform?usp=header**](https://docs.google.com/forms/d/e/1FAIpQLSe7V92eMLFGL6DMX_rz3r1WhvPmD_am9ON-VkE5OfJIDZvbxw/viewform?usp=header)

Q1) Implement the following circuit:

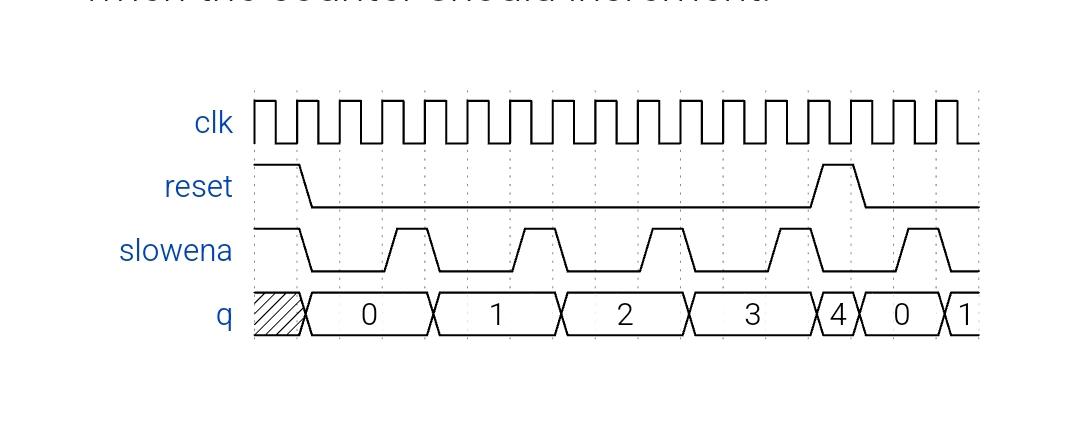


Q2) A SR flip-flop has the below truth table. Implement a SR flip-flop with only a D-type flip-flop and gates. Note: Qold is the output of the D flip-flop before the positive clock edge.

Q3)Imagine you're designing the control system for a digital scoreboard in a basketball game. The scoreboard needs a counter to keep track of points, but with a few specific requirements:

1. Range: The counter should count from 0 to 9 (inclusive) repeatedly.
2. Reset: A special button allows the referee to reset the points to 0 at any time. This reset is synchronized with the clock signal.
3. Pause Functionality: Sometimes, the referee might want to pause the counter instead of updating it with every clock cycle. A control signal (slowena) will determine if the counter should increment on the next clock pulse.

Your task is to design this decade counter for the scoreboard.

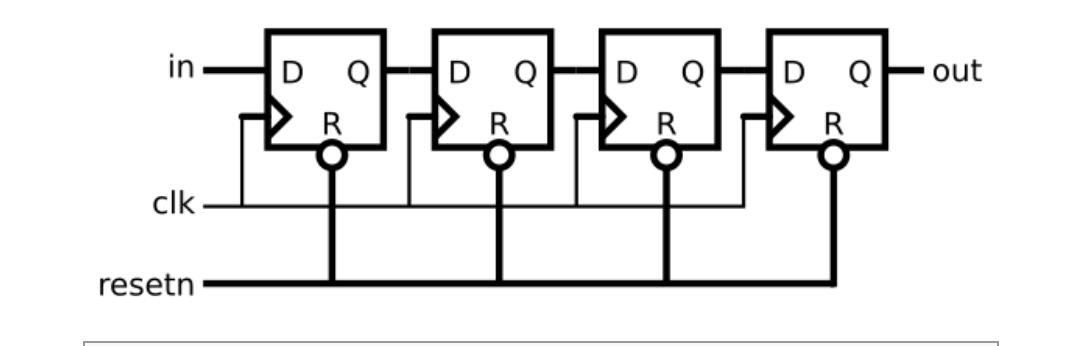


Q4) Build a 4-bit shift register (right shift), with asynchronous reset, synchronous load, and enable.

* areset: Resets shift register to zero.
* load: Loads shift register with data[3:0] instead of shifting.
* ena: Shift right (q[3] becomes zero, q[0] is shifted out and disappears).
* q: The contents of the shift register.

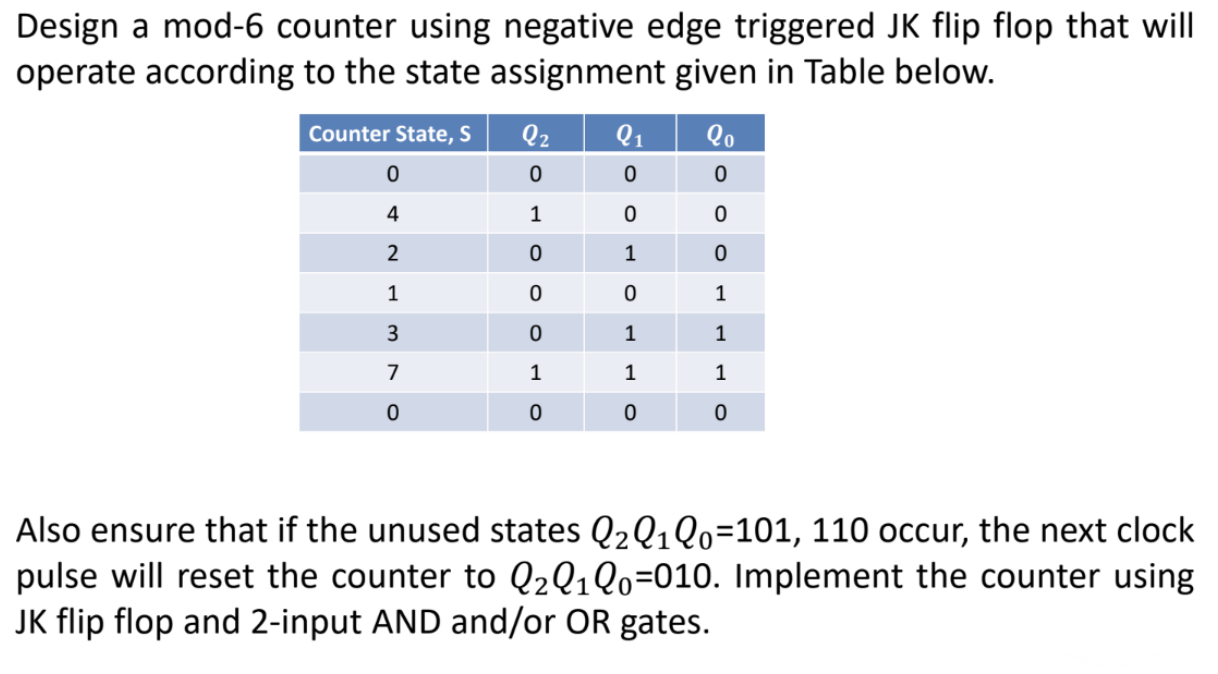
If both the load and ena inputs are asserted (1), the load input has higher priority.

5) Implement the following circuit



6)Design a synchronous counter using D flip flops that goes through the following

repeating sequence 0,2,1,4,3,6,5,7.

7)

8)